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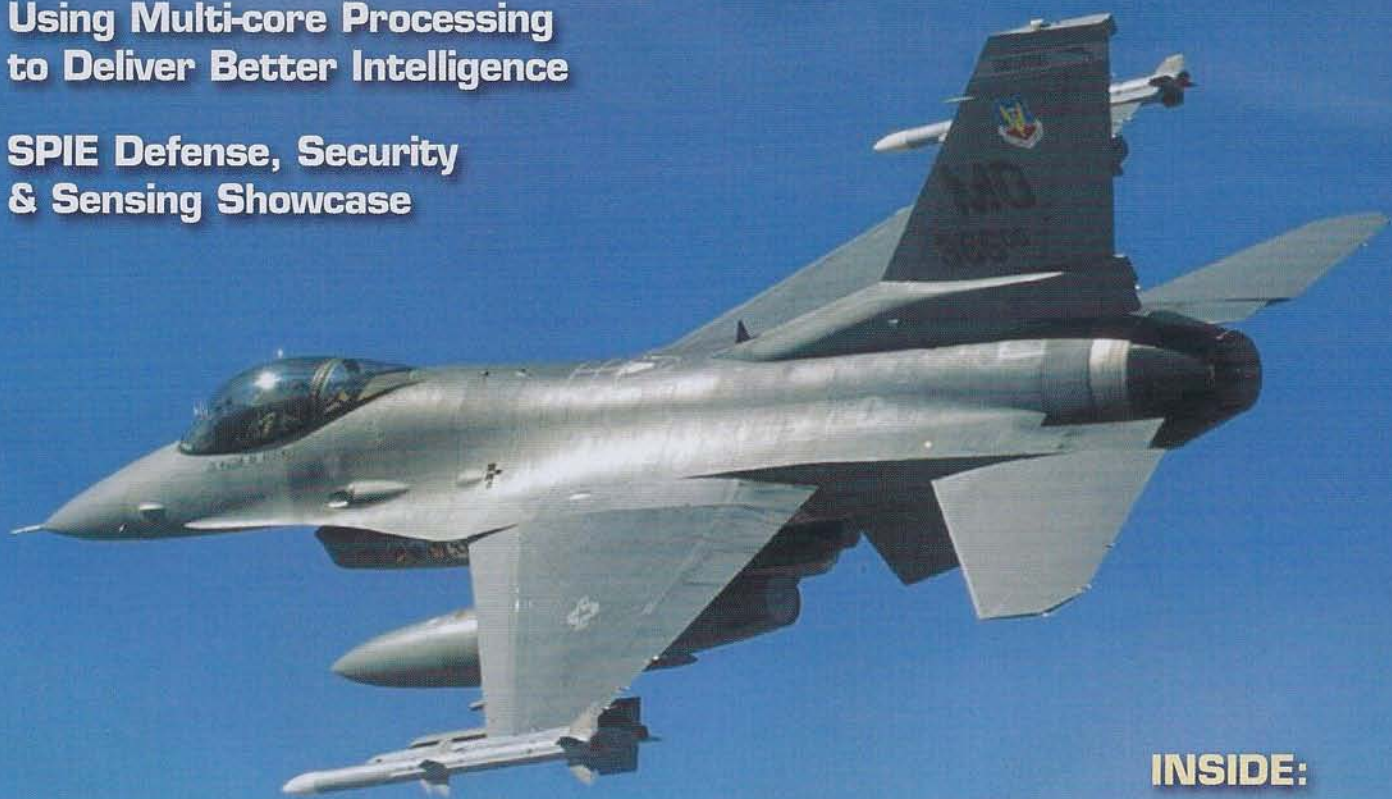
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Using Multi-core Processing to Deliver Better Intelligence

The rapidly evolving and changing asymmetric threats confronting the U.S. military are dramatically escalating demands for intelligence, surveillance, and reconnaissance (ISR). Even unsophisticated countries are gaining access to relatively inexpensive, high technology weapons. In turn, the future weapon systems that low-level tactical units will be combating will be radically improved, and perhaps entirely different than those we attempt to understand today.

To address these volatile threats, the Department of Defense (DoD) is increasingly funding ISR Quick Reaction Capabilities (QRC). This new acquisition model challenges tactical system developers to rapidly deliver cost-effective, high-performance ISR systems while balancing stringent size, weight and power (SWaP) program requirements. In response, ISR system developers are attempting to contain costs, shrink development schedules, and reduce risk as new procurement contracts trend toward fixed-price and away from cost-plus-fixed-fee. These shifts in the military procurement landscape are driving ISR solution providers to leverage pre-integrated, multi-core, commercial-off-the-shelf (COTS) subsystems.

Closing the ISR Collection-Analysis Gap

To keep pace with the outsize demand, the data collection capacity of tactical ISR systems has risen exponentially over the past few years and will continue into the foreseeable future based on the effect of Moore's Law. Even so, ISR data processing, exploitation and dissemination (PED) manning resources have only increased linearly over the same period, leaving a critical gap between collection and analysis capabilities as shown in Figure 1. The outcome is perishable ISR data going unprocessed and/or unexploited and fleeting enemy targets being missed.

To effectively close the ISR collection-analysis gap, the warfighter needs innovative approaches to automate the PED of perishable ISR data to provide mission-critical, real-time actionable intelligence. The harsh reality is that the vast data volumes greatly exceed the ISR sen-

sor platform's ability to transmit the data over bandwidth-constrained wireless communication links in real time. Therefore, the result is likely to be a delay in the remote tactical operations center's high-performance processing, analysis, and fusion.

Automated signal and image processing of ISR data must be performed onboard the sensor platform. By sifting through electronic chaff, the process delivers tactical information that can be transmitted over low-bandwidth communication pipes. Remote, centralized processing stations can then automatically correlate and fuse the data with other ISR sources to provide actionable intelligence to the soldier in the field.

Real-Time Onboard Processing

Pre-integrated, multi-core COTS subsystems provide a viable option for ISR system developers that are looking to cost-effectively integrate high-performance, embedded digital signal processing (DSP) capability on existing ISR collection platforms. Pre-integrated COTS subsystems typically contain

modular embedded processor boards packaged in a rugged enclosure with power supply and interface ports for communication devices or other peripherals. These pre-integrated subsystems can leverage COTS multi-core processing technology to provide high-performance, embedded computing in a very small form factor, while being able to reliably operate in exceedingly harsh tactical environments.

Various COTS vendors such as GE Intelligent Platforms (GE-IP), Mercury Computer Systems, Curtiss-Wright Controls Embedded Computing (CEC), Parvus, and Kontron provide pre-integrated multi-core COTS subsystem products for air, land, and maritime platforms. Figure 2 compares and contrasts key small form-factor, pre-integrated subsystems offered by these COTS product vendors. The table compares the product offerings with respect to performance, SWaP, and ruggedization specifications. These subsystems can be readily integrated into platforms ranging from small UAVs to ultra-quiet submarines to deliver high-performance onboard signal processing.

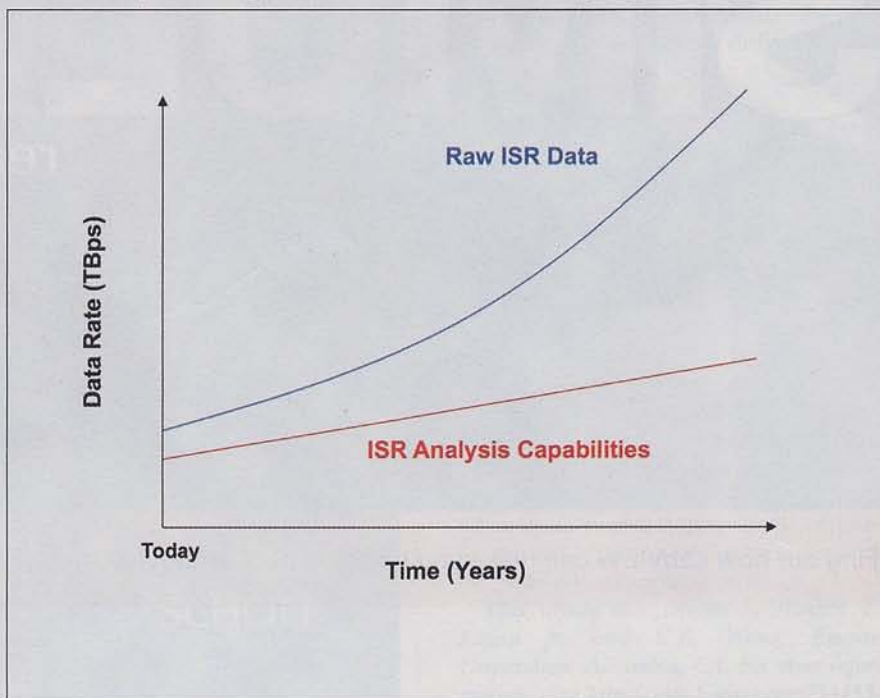


Figure 1. High-performance onboard signal processing helps close the collection-analysis gap.

Using Multi-core Processing

GE-IP and Mercury Computer Systems have embraced the general purpose computing on graphics processing units (GPGPU) paradigm to enable real-time signal and image processing performance onboard a variety of military platforms for high-end ISR applications. GPGPU technology uses graphics processing units with tens or hundreds of processor cores to provide supercomputer-like performance on non-graphical tasks. For rapid application development, environments such as CUDA, OpenCL, ATI Steam SDK, and MATLAB are available to facilitate non-graphical programming tasks.

The GE-IP MAGIC1 rugged embedded computer is a fully, integrated 3U VPX subsystem that includes an NVIDIA GT 240 96-core GPU and an Intel Core™2 Duo processor or a dual core Freescale 8641D for up to 390 GFLOPS of performance. For fanless operation, the MAGIC1 uses an innovative convection cooled thermal design that transfers heat from the unit through integral fins. The small form factor subsystem is designed for severe environment applications with high levels of shock and vibration and temperature extremes in accordance with MIL-STD-810E and MIL-STD-461E. The MAGIC1 is well suited for extremely, high-performance signal, image, and video processing applications on board air, land, and maritime ISR platforms.

The PowerBlock 15 from Mercury Computer Systems is an ultra-compact and lightweight embedded computer optimized for real-time sensor, signal processing, and communications applications. The PowerBlock 15 integrates the Intel Tolapai System-on-a-Chip (SoC) architecture, including the IA-32 core processor, with an AMD M96 GPU to provide up to 350 GFLOPS of processing performance. The subsystem's rugged chassis is designed to isolate its internal electronics from harsh external environmental conditions. At less than 3 lbs, the PowerBlock 15 is ideal for providing high-performance processing on board very lightweight unmanned vehicles.

The primary drawback of the high-performance processing capabilities of the MAGIC1 and PowerBlock 15 is the high power consumption (up to 100 watts). Designers can trade off power consumption for processing speed by adjusting the GPU clocks.

For very low-power ISR applications where small form factor and enhanced onboard signal processing are neces-

sary, COTS vendors such as Kontron, Parvus, and Curtiss-Wright CEC provide multi-core COTS subsystems that can be integrated into even the smallest of UAVs.

The Kontron COBALT (Computer Brick Alternative) is a scalable, high-performance embedded computer. This small, low-profile pre-integrated subsystem provides a fanless, fully enclosed design for efficient thermal management in a small form factor weighing less than 5.5 pounds. The COBALT multi-core option leverages a low power, Intel Core™2 Duo processor system. The rugged embedded computer has been fully qualified against a variety of military environmental test

standards, including MIL-STD-810E and MIL-STD-461E, while providing over 17 GFLOPS of performance. The COBALT is applicable to a wide range of ground vehicle, UAV, airborne or shipboard embedded control and signal processing applications.

The Parvus DuraCor 810-Duo is a rugged, multi-core mission processor subsystem designed for high reliability applications requiring MIL-STD-810G environmental compliance with extreme temperature, shock/vibration, and (humidity, water, and dust) ingress requirements. The DuraCor 810-Duo design leverages a low power, Intel Core™2 Duo processor to deliver up to 12 GFLOPS of signal and image processing performance. The

SFF Multicore COTS Subsystem	Subsystem Performance Parameters			SWaP Parameters			Ruggedization Parameters			
	Multicore CPU	GPGPU Support	Peak System Throughput	Size	Weight	Power	Operating Temperature/ Cooling	Shock/ Vibration	EMI/EMC	Humidity
Kontron COBALT	Intel Core™ 2 Duo (2.2 GHz)	No	17.6 GFLOPS	8.5" x 9.725" x 2.95"	~5.5 lbs	< 25W	-20°C to +55°C Conduction Cooling	Qualified to MIL-STD-810E MIL-S-901D MIL-STD-167	Qualified to MIL-STD-461E	95% non-condensing
Parvus DuraCOR 810-Duo	Intel Core™ 2 Duo (1.5 GHz)	No	12 GFLOPS	10.6" x 5.3" x 5.3"	~8.0 lbs	< 40W	Estimated -40°C to +71°C Conduction Cooling	Designed to MIL-STD-810G	Designed to MIL-STD-461E	95% non-condensing (by analysis)
Curtiss-Wright Controls MPMC-9310	Intel Core™ 2 Duo (1.5 GHz)	No	12 GFLOPS	4.89" x 3.71" x 7.8"	< 5 lbs	< 55W	-40°C to +55°C Convection/ Conduction Cooling	Qualified to MIL-STD-810F	Qualified to MIL-STD-461F	100% non-condensing
Mercury PowerBlock 15	Intel Tolapai SoC with IA-32 Core (1.2 GHz)	Yes - AMD M96 GPU	350 GFLOPS	4.5" x 5.4" x 1.9"	< 5 lbs	< 100W	0°C to +55°C Convection Cooling	Qualified to MIL-STD-810F	Designed to MIL-STD-461F	90% non-condensing
GE-IP MAGIC1	Intel Core™ 2 Duo (2.16 GHz) or Freescale 8641D	Yes - NVIDIA GT 240 GPU	390 GFLOPS	9.05" x 6.57" x 3.25"	~9.5 lbs	< 100W	-40°C to +75°C Convection Cooling	(Shock) 40g peak sawtooth, 11ms duration (vib) Designed to MIL-STD-810E	Designed to MIL-STD-461E	95% non-condensing

Figure 2. Comparison of small form-factor, multi-core COTS subsystem products.

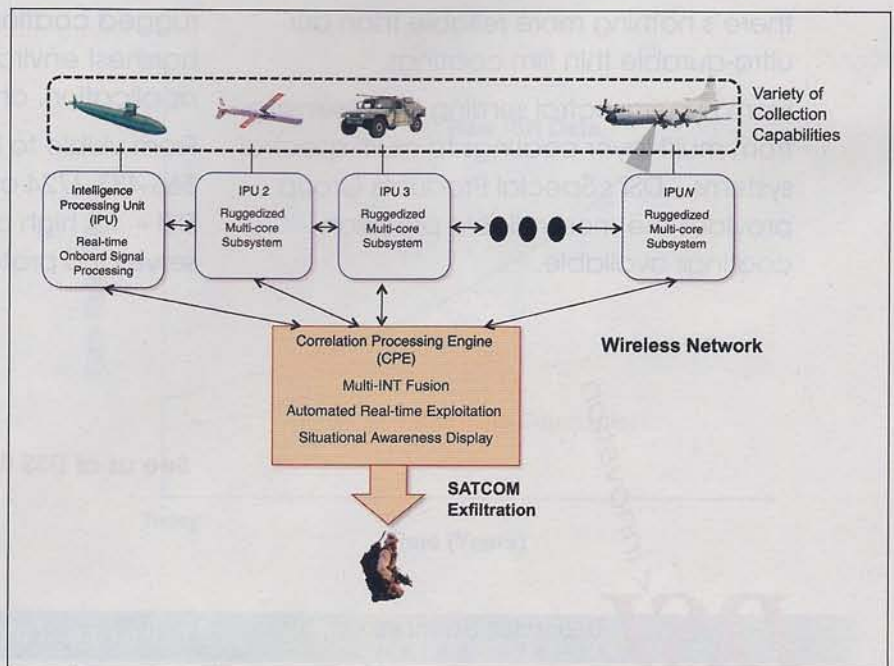
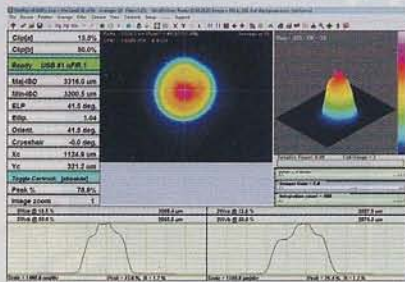


Figure 3. NEOS leverages ruggedized multi-core subsystems to enable real-time PED.

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WinCamD-FIR2-16
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- Wide-bandwidth 2-16 microns profiling
- 2.40 x 2.65 x 1.82" (x 0.9 without filter)
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Using Multi-core Processing



Figure 4. NEOS situational awareness display allows warfighters to easily see threats in real-time.

watertight, conduction-cooled subsystem is designed to meet MIL-STD-461E electromagnetic interference and compatibility (EMI/EMC) requirements. At less than 8 lbs in a man-portable form factor, the unit is well suited for insertion into SWaP-constrained aircraft, ground vehicle, and maritime platform modernization programs.

The Curtiss-Wright Multi-Platform Mission Computer 9310 (MPMC-9310) is a rugged 3U CompactPCI subsystem that supports Intel Core™2 Duo-based single board computers to deliver up to 12 GFLOPS of multi-core performance. The slim profile and light weight (less than 5 lbs) of the MPMC-9310 make it ideal for SWaP-constrained applications such as small UAVs. The subsystem is enclosed in a rugged chassis designed to withstand harsh military environments. The MPMC-9310 is fully qualified against the most stringent military environmental standards, including MIL-STD-810F and MIL-STD-461F. Designed to provide seamless technology refresh on air and land vehicles, the MPMC-9310 provides a viable option for enabling enhanced signal processing onboard these ISR platforms.

Next-Generation Exploitation Optimization System

The IvySys Next-Generation Exploitation Optimization System (NEOS) strongly leverages these ruggedized pre-integrated, multi-core COTS subsystems to provide actionable intelligence to the

warfighter in real time. NEOS is a sensor-agnostic distributed PED system architecture, composed of networked Intelligence Processing Units (IPUs) and Correlation Processing Engines (CPEs). The NEOS IPU is on the collection platform co-resident with multi-modal sensors. Pairing these two components enables real-time compression of sensor data into channelized spectral information and localized sensor correlation and cross cueing using advanced signal processing algorithms. Figure 3 depicts the NEOS real-time PED architecture.

The CPE aggregates information from multiple IPUs to get a global view of the battle space and performs multi-modal sensor fusion and correlation for precision threat detection, classification, identification, geo-location, and tracking. NEOS presents intelligence in an actionable format to the non-technical tactical operator in an easy-to-interpret situational awareness display that provides a Google Map-like view (Figure 4) of the threat environment. NEOS automatically disseminates actionable intelligence to the soldier in the field over potentially low-bandwidth communication links so he or she can make informed, potentially life-saving, decisions in real-time.

This article was written by Dr. James A. DeBardelaben, President and CEO of IvySys Technologies, LLC (Silver Spring, MD). For more information, visit <http://info.hotims.com/34453-521>.